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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,682	08/28/2003	Tetsushi Tanizaki	67161-079	5653

7590 06/13/2006

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600 13th Street, N.W.  
Washington, DC 20005-3096

EXAMINER
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BRITT, CYNTHIA H

ART UNIT	PAPER NUMBER
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2138

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/649,682

Applicant(s)

TANIZAKI, TETSUSHI

Examiner

Cynthia Britt

Art Unit

2138

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☒ Claim(s) 1-5 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>8/28/03</u> . | 6) <input type="checkbox"/> Other: ____.  |

### **DETAILED ACTION**

Claims 1-5 are presented for examination.

#### ***Priority***

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

#### ***Information Disclosure Statement***

The information disclosure statement (IDS) submitted on 8/28/03 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

#### ***Claim Objections***

Claims 1-5 are objected to because of the following informalities:

The following is a quotation of 37 CFR § 1.75(i):

(i.) Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation.

Claims 1-5 are objected to for containing a plurality of elements or steps which are not separated by a line indent. An amendment is required to put the claim in proper format. Line indents aid in understanding the logical grouping of a claim's elements.

Appropriate correction is required.

***Allowable Subject Matter***

Claims 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Providing that the 112 issues in the base claim and any intervening claims of this application have been corrected, these rewritten claims would be allowable.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The following phrase is unclear to the examiner as written “; a boundary scan cell provided corresponding to said terminal and including a first register holding boundary scan test data at the time of said boundary scan test and holding write data to said memory supplied from said terminal at the time of said late write operation in accordance with inactivation of a write control signal”. As there is no clear indication within the claim language, (by either line indents or punctuation) the logical connection between the elements claimed is unclear to the examiner. This should be clarified in order to aid in understanding of the claimed invention. Line indents and punctuation would help in this effort. Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (AAPA) in view of Dreibelbis et al. U.S. Patent No. 5,173,906.

As per claim 1, AAPA teaches "The late write operation is a write operation which is started in response to a rising of a control signal. In the late write operation, upon receipt of data and a write instruction for the data, the device temporarily stores the data in an internal buffer, rather than writing it into a memory cell in a core circuit. Thereafter, the device writes the data held in the internal buffer into a memory cell in the core circuit only when a write instruction for next data is input. The data corresponding to the latter

write instruction is stored in the data buffer, and remains therein until a next write instruction is input". [0005]

Not disclosed by AAPA is the selector and buffer configuration. However, in an analogous art, Dreibelbis et al. teach a boundary scan device for memory testing in which The late write select line depicts when the write address lines should be valid for late write operations. The write gate line shows when the write gate mask lines should be valid. The load compare data line shows the timing for loading of compare data for the respective cycles. Likewise, the result line and load result line depict the timings for the presence of valid result data and the loading. The output is processed from the inputs through a boundary scan and a MUX then to the output through (column 7 lines 45-56 and also, column 8 lines 5-24). Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the output buffers and selectors of Dreibelbis et al. with the AAPA circuitry in order to not lose data.

As per claim 2, Dreibelbis et al. teaches the boundary scan cell receives said boundary scan test data and the output of said input buffer, and said first register holds the output from said input buffer in said late write operation (column 8 lines 5-24 Figures 4 and 13 and related descriptions).

As per claim 3, AAPA teaches input buffer includes a latch circuit which holds the write data input from said terminal in an early write operation in accordance with activation of the write control signal and lets said write data through for output in said late write operation. AAPA [0005]

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"Testing Embedded Memories" by Chuck Plagmann Copyright 1997 Nelson Publishing Inc. <http://www.evaluationengineering.com/archive/articles/1197mem.htm>

This article gives an overview of testing embedded memories and reasons for using various approaches.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
Cynthia Britt  
Examiner  
Art Unit 2138